Grenze International Journal of Engineering and Technology, July Issue

Grid-Voltage Synchronization Algorithms based on Phase-locked Loop for Power Converter under Balanced and Unbalanced Conditions

S.K.Das[1], J.K.Moharana[2] and P Syam[3]
[1, 3] IIEST,Shibpur/Department of EE, Howrah, India
Email: saratkrdas89@gmail.com; prasidsyama@yahoo.co.uk
[2]HIT, Bhubaneswar/Department of EE, Bhubaneswar, India
Emai2: jkrushana@gmail.com

***Abstract*—Rapid integration of non-conventional energy sources connected to grid and distribution systems with electronic power circuits has altered the planned grid specifications to ensure adequate grid failure efficiency. One of the essential control unit's components is phase locked loop(PLL),where power converter grid is connected it. A synchronous reference frame (SRF) PLL approach is proposed in this research for obtaining correct phase knowledge for unbalanced grid voltages. The PLL efficiency was tested for abnormal grid conditions like unbalance, voltage sag, phase jump etc. This paper presents SRF PLL's analysis for the non-ideal grid conditions, where SRF-PLLs are implemented with pre-filters. Exact measurement of grid's fundamental frequency and phase angle is important for grid connected power converter circuit's control algorithm. The pre-filters which are used with SRF-PLL are band pass filter and low pass filter, in which band pass filters can be used to minimize input harmonics and low pass filter can reduce input noise. The implementation has been done through MATLAB software.**

***Index Terms*— Grid Synchronisation, Band pass filter, Low pass filter, Phase locked loop (PLL), total harmonic distortion, PI regulator.**

I. INTRODUCTION

The significance of developing environmentally clean energy sources arises as a result of the growing need to reduce air pollution. Primary sources which do not cause pollution are used for this reason and which are inexhaustible, such as sun, wind, biomass etc. Using these sources means developing more effective electronic power conversion devices which are optimally controlled. The principle of distributed electricity production allows for the linking of small power plants to the grid using renewable energy sources.
In the current scenario, demand of energy is increasing tremendously which in result increase the use of non-conventional energy resources like wind and photovoltaic (PV) for generation of electricity [1]. Photovoltaic needs conversion of DC to AC because power generated from photovoltaic is primarily DC voltage. For AC/DC power conversion, multi-level inverter is currently used in place of conventional inverters because of its some benefits [2]. Continuously, increase of reactive loads and non-linear loads on the grid system which degrades power quality. The number of power quality related problems such as voltage sag, dips, swells and

Grenze ID: 01.GIJET.6.2.513

faults etc. The main operation is to improve the active power injected and to control the Total Harmonic Distortion (THD) within IEEE specifications.
A new concept has been implemented for interfacing grid, such as grid tied inverter which increases the use of power electronics converters. In contrast to synchronous generators with grid synchronization, the inverters don't properly defend to their phase sequencing and phase shift. For that reason the inverters must be integrated with PLL [4] [5]. Grid coordination may raise stability problems, particularly in a weak grids where is high grid impedance; the grid inverter may experience instability because of PLL dynamics & interface of grid impedance[6] [7]. In the case of grid inverter power ratings [8][9], the robustness problems associated with PLL seem to more severe. Refusing to acknowledge the effects of grid synchronisation would cause of its instability [10] [11]. This study provides an optimal PLL can provide the quick and efficient optimization knowledge with a significant level of sag/swells, harmonics, and other distortions of input signal.

II. PHASE-LOCKED LOOP STRUCTURE

The PLL is an algorithm which consist of three main parts namely phase detector, the voltage-controlled oscillator, which changes its output signal phase to match its input period and the loop filter (LF). PLL is the best choice for grid synchronization and control purposes because of its robustness and easy to implement [12]. There is need to extract some information such as phase signal and frequency for monitoring the phase of any signal. The working of phase detector is to match up the incoming reference signal and the signals' phase from voltage controlled oscillator (VCO) and it produces error voltage. The phase detector's error Voltage is proportional to phase difference of input signal and internal oscillator signal produced by PLL. The error signal moves through a low pass filter. Low pass filter handles many of the loop's properties, and keeps the loop stable. It also eliminates any components with high frequencies on the signal. Low pass filter makes an attempt to keep the difference in phase at a minimum level and also keep the frequency between the two input signals [13]. The loop will be out of lock at the initial stage of the PLL, and the error voltage will move the VCO frequency to the reference voltage until the error can be minimized and the loop fixed.
One form of PLL is the detection of zero crossing which determines frequency or periodic signal cycle. The reference signal cycles is usually estimated over one or more time periods of the measured signal, while calculating signal's frequency. Sampling many phases helps to reduce the errors caused by phase noise by reducing the variations in zero crossings compared to the total time of observation. The net result is accurate assessment at the cost of slow estimating levels [14]. ZCD has benefits of easily simulated but it fails to operate when pass through multi-zero-crossing and it also having drawback of weak dynamic response because of control over one cycle or half cycle [15].
On the other hand, during an unbalanced voltage state the stationary PLL structure based reference frame is not capable of accurate phase monitoring. Seeing as grid connected systems experience problems like shift input step, dip, notch, flicker, and difference in amplitude etc [16]. The SRF PLL is among the three provides more than good result under skewed and non-ideal grid circumstances [17] and therefore this study followed the synchronous rotating reference frame (SRF) based PLL design approach to build a model which suitable for synchronizing a DG with the grid under numerous disruptions to improve the quality of the electricity.
We need to monitor the phase angle, because of synchronization of grid. For monitoring phase angle two methods are present i.e. open loop methods (OL) and closed loop methods (CL) [18].The space vector filters or extended Kalman filters and the low pass filters are few filters which we can use in open loop methods. Such approaches will estimate PCC voltage's phase angle directly from the Clarke transformation of its alpha and beta coordinates [19]. PLL is regarded as the key tool in CL methods & used in phase angle's true value monitoring. In PLL the phase angle measurement is rationalized regularly using a CL mechanism [20]. This approach also has some demerits, like, not functioning properly under frequency changes and imbalances. In current era to tackle such drawbacks a new kind of PLL is introduced. The key objectives of these approaches of PLLs are to provide robust response under imbalance input signal and harmonics signal. Both strategies can also be taken for a 3-Ø power conversion system under non ideal condition. This system's control phase is very complicated and therefore requires heavy computing stages [21].
There are many approaches of estimating grid voltage's phase angle for getting inverter's voltage compatibility with the 3-Ø grid voltages. For grid synchronisation, various kinds of synchronization approaches are performed. These comprise of Synchronous Reference Frame (SRF) PLL, Dual Second Order Generalized Phase-Lock Loop (DSOGI) PLL, Multiple Second Order Generalized (MSOGI) Frequency-Lock Loop (FLL) and Positive Sequence Detector (PSD) based dq -PLL [22]. Above mentioned strategies

have their own benefits and drawbacks. SRF-PLL is a much efficient control technique amongst the various control techniques. All of these strategies may be used in various non-conventional energy applications and the corresponding control strategy which is suited for particular application may depend on the specifications and regulations to be met for grid interfacing.

A. Stationary Reference Frame V_α ***and*** V_β

In stationary reference frame the 3-Ø voltage signals (V_a, V_b, V_c) transformed to stationary network which comprises of 2-Ø voltage $(V_\alpha \ \& V_\beta)$ to calculate the phase angle. The grid's voltages are mentioned below,

$$V_a = V_m \sin(\theta) \quad (1)$$

$$V_b = V_m \sin(\theta - \tfrac{2\pi}{3}) \quad (2)$$

$$V_c = V_m \sin(\theta + \tfrac{2\pi}{3}) \quad (3)$$

Where, θ is the angle of phase having value 2πft. The eq.(4)illustrates the αβ-transformation matrix.

$$T_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \quad (4)$$

The matrix multiplication $V_{\alpha\beta} = T_{\alpha\beta} V_{abc}$ as shown in eq. (5) which have two signals but phase angle information of one phase only, 'Va'.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} V_m \sin(\theta) \\ V_m \cos(\theta) \end{bmatrix} \quad (5)$$

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B. Synchronous rotating reference frame

The angle of phase is evaluated is done with space vector synchronization of voltage along SRF's d or q axis. Fig.1 depicted that the space vector of voltage correspond to the axis of q.

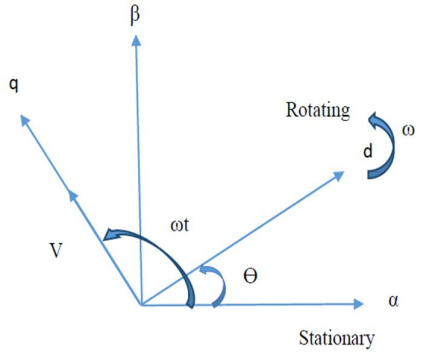

Fig.1: Synchronous rotating reference frame

To synchronize the voltage space vector with the axis of q, the transformation matrix is

$$T_{qd} = \begin{bmatrix} \sin\theta^* & \cos\theta^* \\ -\cos\theta^* & \sin\theta^* \end{bmatrix} \quad (6)$$

Where, θ^* is the PLL system's estimated output of phase angle. Carrying out the transformation $V_{qd} = T_{qd} V_{\alpha\beta}$ and using the trigonometric addition the formulas as given in equation (7).

$$\begin{bmatrix} V_q \\ V_d \end{bmatrix} = \begin{bmatrix} V_m \cos(\theta - \theta^*) \\ -V_m \sin(\theta - \theta^*) \end{bmatrix} \quad (7)$$

The angle of phase 'θ' is estimated with θ* and it is the integral of the estimated frequency 'ω'. The estimated frequency 'ω' is the sum of the feed forward frequency 'ω_{ff}' and the PI-output. PI-regulator's gain

is then designed so that V_d follows the reference value $V_d^* = 0$, as depicted in fig.2. To synchronize the voltage space vector with the q-axis the value of V_d should be zero & the measured frequency 'ω' is locked. The correspondent result of calculated phase angle θ* equals to the phase angle θ.

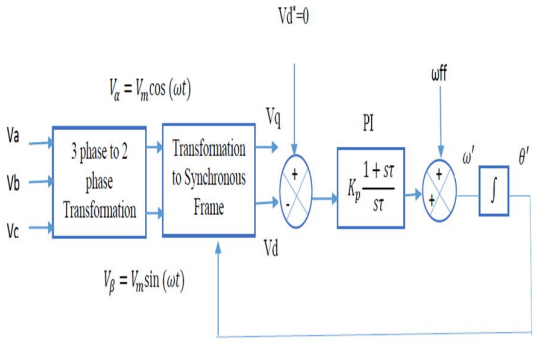

Fig.2: SRF- PLL Structure

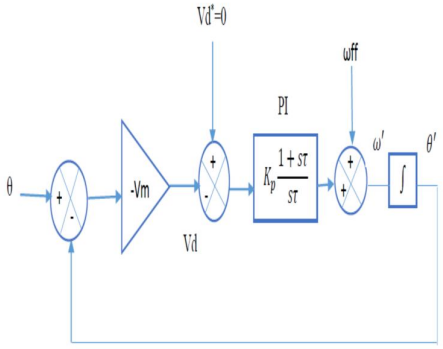

Fig.3: Modified SRF- PLL

If θ* ≈ θ then the minute angle approximation for sinus function gives $V_d = -V_m(\theta - \theta^*)$ and the structure of SRF-PLL is shown in fig. 2 can be modified, as depicted in fig. 3 which equals to the phase angle θ. The feed forward frequency is to have the PI-regulator power for an output signal that goes to null value. In this case the frequency of feed forward will be 2πf. Ideally for the grid frequency is exact 50Hz once the regulator has been monitored, the output of the regulator process is zero.

III. Proportional- Integral Controller

The PI controller is typically taken to suppress the error of steady state arising from the proportional controller. In addition, the overall system reliability has a negative impact as regards response time. This controller is often taken in those circumstances where system speed is not concern. As PI controller does not have the ability to predict potential system failures; it can't increase or reduce the rise time with oscillations removal. Any degree of integration, if applicable, guarantees overshoot of the set point [23] [24].

A. PI Regulator Gains Design

There are different ways to create specification of PI regulator. The best approach based on the regulator criteria. We have second-order system and the symmetrical optimum method (SO) used in most of the PLL grid connecting applications which is an effective approach to use. The transfer function of system is

$$G = K_p\left(\frac{1+s\tau}{s\tau}\right)\left(\frac{1}{1+sT_s}\right) \quad (8)$$

The SRF PLL's open-loop transfer function is

$$G_{ol} = K_p\left(\frac{1+s\tau}{s\tau}\right)\left(\frac{1}{1+sT_s}\right)\left(\frac{V_m}{s}\right) \quad (9)$$

The SRF PLL's closed-loop transfer function is

$$G_{cl} = \frac{G_{ol}}{1+G_{ol}} \quad (10)$$

Eq. (11) defines the relation between Z domain and S domain

$$s = \frac{z-1}{T_s} \quad (11)$$

The symmetric optimum method transfer function is

$$G = \frac{\omega_0^2(ks+\omega_0)}{s^2(s+k\omega_0)} \quad (12)$$

By correlating symmetric optimum (SO) method's transfer function & open loop transfer function giving following descriptions:

$$\omega_c = \frac{1}{aT_s}$$
$$\tau = a^2 T_s \quad (13)$$
$$k = \frac{1}{aV_m s}$$

Regulator outcomes gain by SO approach. A cross over frequency can be selected for the sampling time period of Ts = 100 μs and by changing the normalizing factor.
Cross-over frequency and bandwidth for second-order system was planned using simulations of limited space in the signal state. If the phase margin is more, then the oscillation response is less, lower s value reduces both phase margin and bandwidth settling time and gain impact value.

B. Attributes of the framework

The inverter grid voltage is 1000V which is rms value of the line-to-line voltage at the grid connection point. The amplitude voltage level 'V_m', is then calculated considering 3-Ø voltage in a SRF using V = 816V, corresponding crossover frequency 50Hz & Ts = 0.5ms as shown in eq. (13) as,

$$\begin{Bmatrix} a = 6.3662 \\ \tau = 0.0203 \\ K_p = 0.3848 \end{Bmatrix} \qquad (14)$$

By putting the values of eq. (14) in eq. (9) we get the OL system's TF & from this transfer-function, system bode plot diagram is illustrated. The balanced form is reported from the bode plot and the phase margin is ψ = 72.1 degrees at the crossover frequency 'ω_c' = 314 rad/s, as depicted in figure 4. The closed loop system transfer function can be evaluated using equation (10). A bode plot of the CL system depicts the system behaviour as a low pass filter as shown in figure 5.

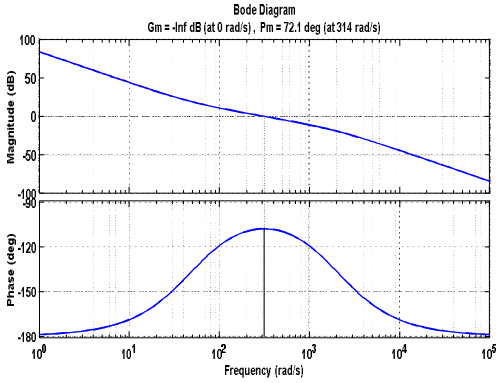

Fig.4: Open loop system bode plot

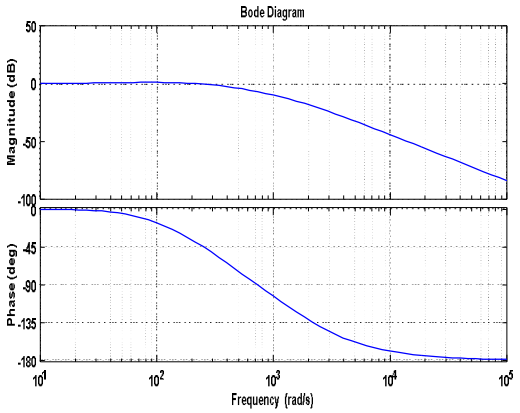

Fig. 5: Closed-loop system bode plot

IV. PROPOSED SRF-PLL

In the proposed approach the SRF-PLL is simulated with pre filters and it is made for giving robust result under non-ideal grid condition during grid synchronization. In the non-ideal condition harmonic in the input signal occurs with the large frequency range, the traditional PLL methods can't obtain accurate phase information. New SRF-PLL method has been developed for 3-Ø grid connected inverter systems.
The Fig.6 shows the MATLAB/Simulink model that proposes SRF-PLL. In this 3-Ø voltage signals (V_a, V_b, V_c) are transferred from 3-Ø to 2-Ø stationary system $(V_d \ \& V_q)$. Such q_e and d_e variant are obtained by V_d and V_q variant. For extracting the basic signal from grid voltage a low pass filter is built and is taken as a unity sine reference which is extracted by the block of conversion q_e to the block of generations of signals sin-cos. This sin-cos signal is fed back to the conversion unit for locking the phase angle and frequency between voltage of grid and angle of phase.
PI regulator function in this PLL circuit is to record the phase for changed grid frequencies (either less or more with comparison of rated frequency).The pre-filters such as low pass filter and band pass filter are used in proposed methodology. These practices to decrease harmonics presence in input voltage. The pre-filters are placed before the synchronous frame transformation.

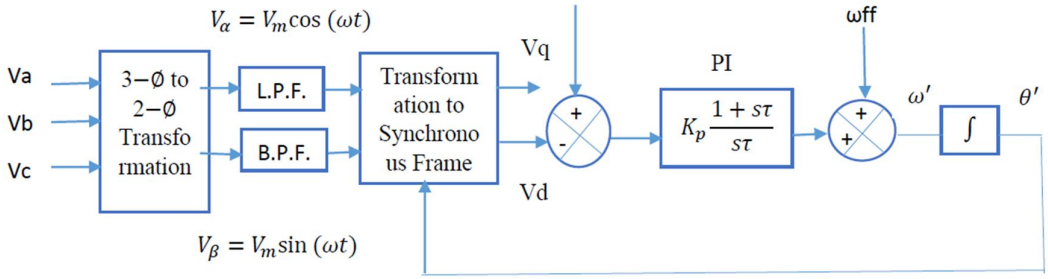

Fig.6: Proposed SRF PLL block diagram

The complete model explanation of the system in MATLAB/Simulink software with PI regulator is simulated. For 1 kV rms grid voltage the PT regulator is implemented. The main input voltage is V_{abc} in the system which is transformed into dq transformation using coordinate transformation $abc - dq$. In this transformation only V_q is taken and V_d^* is set to zero. The discrete transfer block introduce PI regulator gain, which suppress the portion of high frequency & provide the voltage controlled oscillator (VCO) with DC controlled signal(acts as an integrator, represented by the discrete-time integrator block). The output of PI controller is output frequency of the inverter combined for determining the phase angle of the inverter. While difference between the phase angle of grid and inverter's phase angle is reduced to zero & PLL will becomes active resulting in synchronously rotating voltages $V_d = 0$ and magnitude of grid voltage is shown with V_q.

V. Result and Discussion

There are following state to simulate model for non-linear condition:

A. Non-ideal state

The PLL is generally a phase-tracking technique. As the need of perfect sine wave but the PLL is not able to satisfactorily operate in distorted and non-ideal condition. Non-ideal conditions of 3-Ø system are harmonics presence, unbalanced amplitudes, variation in frequency and phase jump. Due to some reason, such type of conditions occurs in the system. When a generator is connected or disconnected to the grid which produces the phase-jump and non-linear load or transformer produces harmonics in grid voltages. This will display the grid's reaction to some disruptions, and the PLL's ability to address those disturbances. Such disturbances are defined as follows-

B. Harmonics

In the input signal, the 5th, 7th and 11th harmonic with amplitude of 10 percent, 8 percent and 5 percent of V_m respectively added. Fast Fourier Transform (FFT) is measured to evaluate signal frequency spectra. Throughout this manner, the harmonics effect in the input and output signal can be compared, which is depicted in figure 7 (a) and 7 (b).

C. Voltage Sag

Voltage sag is a drop in voltage for a short period. It is happened because of short-circuit, starting of electric motors and large loads are plugged into or isolated from the grid. Voltage sag occurs when the reduction in rms voltage between 10-90% of specified voltage for 0.5 cycle to 1 minute. In this work, 30 percent reduction in 3-Ø voltage is shown in figure 8.

D. Phase jump

The sudden change in phase of system voltage due to short-circuit or disconnect of large loads from the source, this phenomenon is called phase jump. Phase jump in the input signal as shown in fig 9.The input signals with phase jump are applied at the simultaneously with 3-Ø as shown in fig.9.

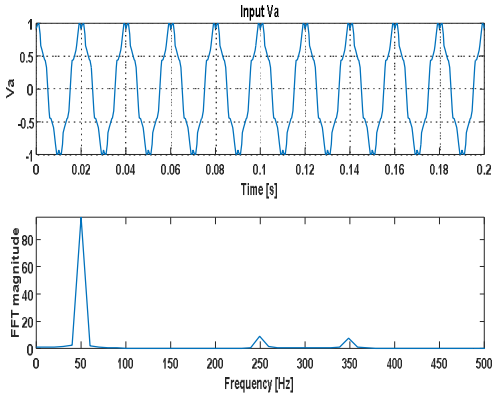

Fig.7 (a): Frequency spectra and Input signal with harmonics

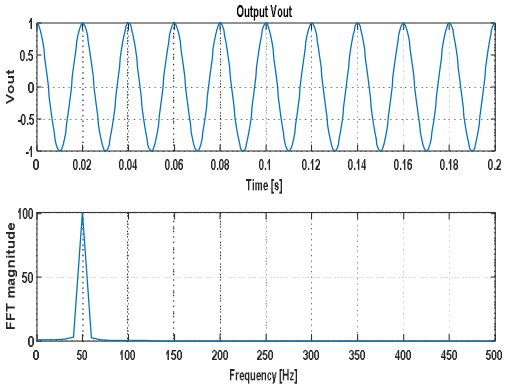

Fig.7(b): Frequency spectra and output signal

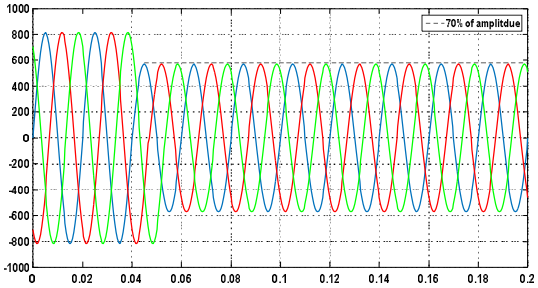

Fig.8: Reduction in amplitude of input voltage

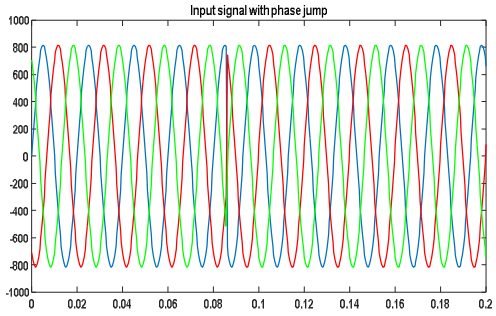

Fig.9: Phase Jump in input voltage

E. Unbalanced amplitudes in input signal

Fig. 10 shows the performance of PLL system under unbalanced conditions. The PLL system is applied during unbalanced input signal of 3-Ø system with the value of V_b is 0.85*V, V_c is 1.15*V and value of V_a is unchanged.

F. Unbalance frequencies in input signal

In the three phase system, V_a input signal having frequency of 50Hz, V_b input signal having frequency of 48.5 Hz and V_c input signal having frequency of 51.5 Hz as depicted in figure 11.

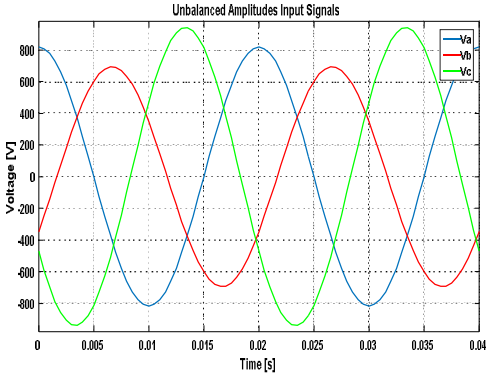

Fig.10: Unbalanced amplitudes in input signal

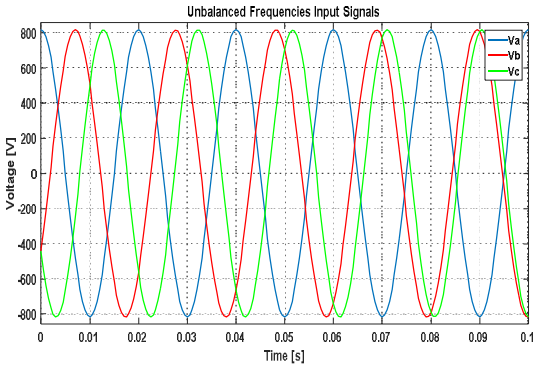

Fig.11: Unbalance frequencies in input signal

VI. Conclusion

For tracking grid phase angle a SRF-PLL has been implemented in MATLAB/Simulink. For non-ideal condition the proposed SRF-PLL is could coordinate the non-conventional energy sources to the grid. The PLL method has less fluctuations and a high ability to reject errors, which implies reliability and enhanced response speed. The proposed approach has less fluctuations and a high ability to reject errors, which implies reliability and enhanced response speed.

The mechanism simply acts as a low pass filter when harmonics are present in the input signals and the impact of the harmonics in the output signal is reduced. The system handles phase jumps without any difficulties. We find out that the proposed approach is able for non-ideal condition with the cost of loss in accuracy and PLL with PI regulator gain is tracked phase angle in acceptable margin. So, it could be operate in real life application. To make the system more dynamic, the value of τ should be lower.

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